EXHIBIT 21

[redacted]

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VIA ELECTRONIC MAIL

October 20, 2023

Mr. Jason Sheasby, Esq.
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1800 Avenue of the Stars, Suite 900
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Re: *Netlist v. Samsung*, No. 22-cv-293 (E.D. Tex.) – Netlist's Deficient Response to Interrogatory No. 17

Counsel:

I write regarding deficiencies in Netlist's response to Samsung's Interrogatory No. 17, which requests Netlist "identify and describe in complete detail all factual and legal bases for [Netlist's] disagreement with [Samsung's] contentions that the Asserted Claims are invalid under 35 U.S.C. §§ 102, 103, and/or 112, including all support for such disagreement, any claim elements You allege are not disclosed by the prior art, and why each of the disclosed references and systems and the disclosed combinations thereof do not anticipate or render obvious the Asserted Claims on a claim element-by-claim element basis."

At present, Netlist only provides a boilerplate response that Samsung bears the burden of proving invalidity, "no single reference anticipated the Asserted Claims, no single reference or combination of references renders the Asserted Claims obvious, the Asserted Patents identify the proper inventors of the subject matter sought to be patented by the Asserted Claims, the specifications of the Asserted Patents contain adequate written description for the Asserted Patents, and the specifications of the Asserted Patents enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and set for the best mode contemplated by the inventor for carrying out the invention." Netlist further states that it "will provide Samsung with its validity expert report(s) and supporting documents according to deadlines set in this Court's Docket Control Order for expert report and discovery."

Netlist's response is insufficient, as it fails to provide any specific information about Netlist's disagreements with Samsung's invalidity contentions, including any element Netlist contends is not disclosed by the prior art or combinations thereof or any identification of the sections of the specification that provide written description support for the Asserted Claims.

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Netlist's response fails to explain how the specifications of the Asserted Patents provide support for the claim elements that Samsung identified in its contentions as failing to satisfy the written description requirement. As reflected in Samsung's invalidity contentions, the Asserted Patents include numerous claim elements that are not properly supported in Netlist's patent specifications. I provide examples below for which we have not received any response:

- Netlist's response fails to explain how the specification of the '215 patent provides written description support for control signals sent to a buffer to enable communication of a data burst between at least one first memory integrated circuit and a memory controller through the buffer in response to a memory command where the same memory command is also received and buffered by a register. As part of Netlist's supplemental response, Netlist needs to specifically and separately identify the written description support by identifying the column, line number, drawing, and drawing reference number, if any, for each of the following claim limitations and describe the basis for any contention that such claim element is disclosed by the specification of the patent: (a) the "first command and address signals representing the first memory command"; (b) the "first memory command" being "receive[d] and buffer[ed]" by a "register"; and (c) "logic … configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer." *See* '215 patent at claim 1.

- Netlist's response fails to explain how the specification of the '215 patent provides written description support for first control signals to a buffer to enable communication of a first data burst and second control signals to the buffer to enable communication of a second data burst where the second control signals are different from the first control signals. As part of Netlist's supplemental response, Netlist needs to specifically and separately identify the written description support by identifying the column, line number, drawing, and drawing reference number, if any, for each of the following claim limitations and describe the basis for any contention that such claim element is disclosed by the specification of the patent: (a) "first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"; (b) "second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer;" and (c) "the second control signals being different from the first control signals." *See* '215 patent at claims 1 and 21.

- Netlist's response fails to explain how the specification of the '417 patent provides written description support for "logic … configurable to output data buffer control signals in response to the read or write memory command." As part of Netlist's

supplemental response, Netlist needs to specifically and separately identify the written description support by identifying the column, line number, drawing, and drawing reference number, if any, for each of the following claim limitations and describe the basis for any contention that such claim element is disclosed by the specification of the patent: (a) "logic … configurable to output data buffer control signals"; (b) the "data buffer control signals"; (c) a "read or write memory command"; and (d) "data buffer control signals in response to the read or write memory command." *See* '417 patent at claim 1.

- Netlist's response fails to explain how the specification of the '417 patent provides written description support for logic that i) receives a set of input address and control signals associated with a read or write memory command via the address and control signal lines wherein the set of input address and control signals including a plurality of input chip select signals and other input address and control signals; ii) outputs a set of registered address and control signals in response to the set of input address and control signals wherein the set of registered address and control signals includes a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals; and iii) outputs data buffer control signals in response to a read or write memory command. As part of Netlist's supplemental response, Netlist needs to specifically and separately identify the written description support by identifying the column, line number, drawing, and drawing reference number, if any, for each of the following claim limitations and describe the basis for any contention that such claim element is disclosed by the specification of the patent: (a) "logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines"; (b) "logic … to output a set of registered address and control signals in response to the set of input address and control signals"; (c) "the set of input address and control signals including a plurality of input chip select signals and other input address and control signals"; (d) "the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals"; (e) "wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command"; (e) "memory devices … arranged in a plurality of N-bit wide ranks… wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command"; (f) "circuitry … configurable to transfer the burst of N-bit wide data signals … in response to the data buffer control signals." *See* '417 patent at claim 1.

- Netlist's response fails to explain how the specification of the '215 patent and the specification of the '417 patent provide written description support for a data buffer without a fork-in-the-road, *i.e.*, two output data lines selectively electrically coupled to a single input. As part of Netlist's supplemental response, Netlist needs to specifically and separately identify the written description support in each patent specification by identifying the column, line number, drawing, and drawing reference number for the following limitations that Netlist claims are sufficiently broad to include a data buffer without a fork-in-the-road: "logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer" ('215 patent, claim 1), "wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals" ('215 patent, claim 1), "providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer" ('215 patent, claim 21), "providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer" ('215 patent, claim 21), "circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module" ('417 patent, claim 1).

- Netlist's response fails to explain how the specification of the '417 patent provides written description support for circuitry constituting multiple data buffers for transmitting N-bit wide data signals. As part of Netlist's supplemental response, Netlist needs to specifically and separately identify the written description support in each patent specification by identifying the column, line number, drawing, and drawing reference number for the following limitation that Netlist claims is sufficiently broad to include circuity with multiple data buffers for transmitting N-bit wide data signals: "circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module." *See* '417 patent at claim 1.

- Netlist's response fails to explain how the specification of the '608 patent provides written description support for "a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit." As part of Netlist's supplemental response, Netlist needs to specifically and separately identify the written description support by identifying the column, line number, drawing, and drawing reference number, if any, for each of the following claim limitations and describe the basis for any contention that such claim element is disclosed by the specification of the patent: (a) "a command processing circuit configured to decode the module control signals", (b) "a command processing circuit configured . . . to control the data path in accordance with the module control signals and the module clock signal," (c) "at least one tristate buffer," and (d) "controlled by the command processing circuit." *See* '608 patent at claim 1.

- Netlist's response fails to explain how the specification of the '912 patent provides written description support for "the set of input signals configured to control a second number of DDR [memory/DRAM] devices." As part of Netlist's supplemental response, Netlist needs to specifically and separately identify the written description support by identifying the column, line number, drawing, and drawing reference number, if any, for each of the following claim limitations and describe the basis for any contention that such claim element is disclosed by the specification of the patent: (a) "first number of DDR memory devices arranged in a first number of ranks"; and (b) "the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks"; and (c) "the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks." *See* '912 patent at claim 16.

- Netlist's response fails to explain how the specification of the '912 patent provides written description support for "the command signal is transmitted to only one DDR memory device at a time," particularly under Netlist's construction of "rank" as requiring multiple memory devices. As part of Netlist's supplemental response, Netlist needs to specifically and separately identify the written description support by identifying the column, line number, drawing, and drawing reference number, if any, for each of the following claim limitations and describe the basis for any contention that such claim element is disclosed by the specification of the patent: (a) "command signal"; and (b) transmission of the command signal "to only one DDR memory device at a time." If Netlist contends that the '912 patent provides written description support for selection of individual memory devices within a multi-device "rank," Netlist's response should further identify the column, line number, drawing, and drawing reference

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number, if any, allegedly corresponding to that functionality. *See* '912 patent at claim 16.

Please confirm by October 27, 2023, that Netlist will supplement its response to Interrogatory No. 17 to address the issues noted in this letter.

Sincerely,

Daniel A. Tishman

cc: All counsel of record